



INDIAN INSTITUTE OF TECHNOLOGY PATNA
BIHTA PATNA-801106
RESEARCH & DEVELOPMENT UNIT

ADVERTISEMENT NO: R&D/908/MEM/405
Project No. R&D/SP/EE/MEM/2023-24/908

DATED: 05.09.2024

Applications are invited in the prescribed format only for the following assignment in a purely time bound research project undertaken in this institute.

1. (a) Name of the temporary assignment: Junior Research Fellow (JRF)

(b) Number of Post : 02 (Two)

(c) Duration of the Post : 02 (Two Years) as JRF, thereafter Senior Research Fellow (SRF) till completion of the project

(d) Duration of the Project : Four Year (May extend to another one year)

2. Name of the temporary research project : ML Enabled RISC-V based i-LoRa SOC for Forest Event Monitoring

3. Name of the sponsoring Agency: Ministry of Electronics and Information Technology (MeitY), Delhi under C2S Programme

4. Consolidated Fellowship/Salary: Rs. 37000 (for JRF) and Rs. 42000 (for SRF)

5. Qualification : M. Tech./B. Tech./M.Sc. (Electrical /Electronics/Communication/ Instrumentation / Computer Science & Engineering)

The candidate desirably should have **M.Tech.**(VLSI/Embedded System/Microelectronics/Electronics System/Communication System/Computer Science Engineering/Allied discipline) degree with a minimum CPI of 7.0 or 70% of marks with qualified GATE Score (within last five years) **ORB.Tech/B.Sc(Engg.)/M.Sc.**(Electrical/Electronics/Communication/Instrumentation/Computer Science & Engineering) degree with a minimum CPI of 7.5 or 75% of marks with qualified GATE Score (within last five years). GATE score shall be exempted for candidates having B.Tech degree with minimum CPI 7.0 from IITs. Exceptional candidates having M. Tech degree and minimum two (02) years of relevant experience, may be offered SRF Position directly based on the performance in interview. The upper age limit for applying for the JRF position shall be **32 and 28 years** for candidates having M.Tech and B.Tech/B.Sc.(Engg.)/M.Sc. degree respectively on the date of advertisement.

Relaxations for SC/ST/OBC/women/PD will be given as per the GOI rules. Working/research experience in the field of **VLSI and Embedded System/ Computer Architecture/ Communication System/Machine Learning and exposure to EDA tools** shall be given preference.



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Interested and eligible candidates may send the scan copy of **application form(in appended format) and GATE Score Card** along with **resume** highlighting the relevant exposure in the domain of the project to the mail id: kcr@iitp.ac.in. on or before **3rd Oct. 2024**. Shortlisted candidates shall be intimated on **4th October 2024** and called for the **PERSONAL INTERVIEW(Hybrid mode)** to be scheduled on **15th October 2024**, Timing **10 AM** at Dept. of Electrical Engineering, IIT Patna, Bihta, Patna – 801103 with updated resume along with the original copies of all supporting documents (certificates, mark-sheets, and GATE Score card).

No TA/DA is admissible for appearing in the interview. Guest room in student hostel may be arranged on prior intimation through mail for maximum two days only.

Important Dates:

Last date for receiving the application form through mail: 3rd October 2024

Date of intimation of shortlisted candidates through mail: 4th October 2024

Date of Personal Interview : 15th October 2024

Please Note that, candidates those are willing to pursue PhD in Electrical Engineering Department starting from January 2025 session, are only encouraged to apply this JRF/SRF position subject to the fulfil of the PhD admission protocol of the department and institute.

For any query, please contact Principal Investigator of the Project: **Dr. Kailash Chandra Ray**, Dept. of Electrical Engineering, IIT Patna, Email: kcr@iitp.ac.in. Tel.: 06115-233106 (Office).

Deputy Registrar

Copy to:

1. Associate Dean, R&D, IIT Patna
2. Advertisement file
3. Project file